



MCS7840

High Speed USB to Quad - Serial Port

Application Note for Custom baud rates

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Revision History

Name	Date	Reason For rewrite	Version
AJN	20 th Jan 2007	Initial release	1.0

Introduction & Overview

The MCS7840 is a High Speed USB to Quad Serial Port device. It has been developed to connect a wide range of standard serial devices to a USB host. This application note describes the ways to set baud rates. It also describes how to set the non-Standard baud rates with MCS7840 device.

The major blocks in the serial baud rate clock generation are PLL, Clock Recovery and Clock Generation Blocks. These blocks are responsible for setting the desired baud rate of each serial port individually.

a) Default mode / Standard baud rates :

Following baud rates supported with default settings of Driver :

Baud Rate (Bits per Second)	Clock recovery out(MHz)	Baud Clock Logic Out(Hz)	DLAB Bits	
			DLM	DLL
50	1.8432	798.6	9	0
75	1.8432	1.1979K	6	0
110	1.8432	1.757K	4	23
134	1.8432	2.147K	3	89
150	1.8432	2.395K	3	0
300	1.8432	4.791K	1	128
600	1.8432	9.583K	0	192
1200	1.8432	19.160K	0	96
1800	1.8432	28.750K	0	64
2000	1.8432	31.724K	0	58
2400	1.8432	38.33K	0	48
4800	1.8432	76.666K	0	24
7200	1.8432	115K	0	16
9600	1.8432	153.33K	0	12
14400	1.8432	230.4 K	0	8
28800	1.8432	307.2K	0	6
19200	1.8432	460.8K	0	4
38400	1.8432	613.33K	0	3
57600	1.8432	920 K	0	2
115200	1.8432	1.84 M	0	1

Baud Rate (Bits per Second)	Clock recovery out(MHz)	Baud Clock Logic Out(Hz)	DLAB Bits	
			DLM	DLL
230400	3.6864		0	1
460800	7.3728		0	1
921600	14.7456		0	1

Following baud rates can be supported by setting “Enable High Baud” setting Under Serial port settings :

Baud Rate (Bits per Second)	Clock recovery out(MHz)	Baud Clock Logic Out(Hz)	DLAB Bits	
			DLM	DLL
1.5M	24		0	1
3.0M	48		0	1
6.0M	96		0	1

403200 & 806400 bps baud rates are also supported under standard baud rate support table.

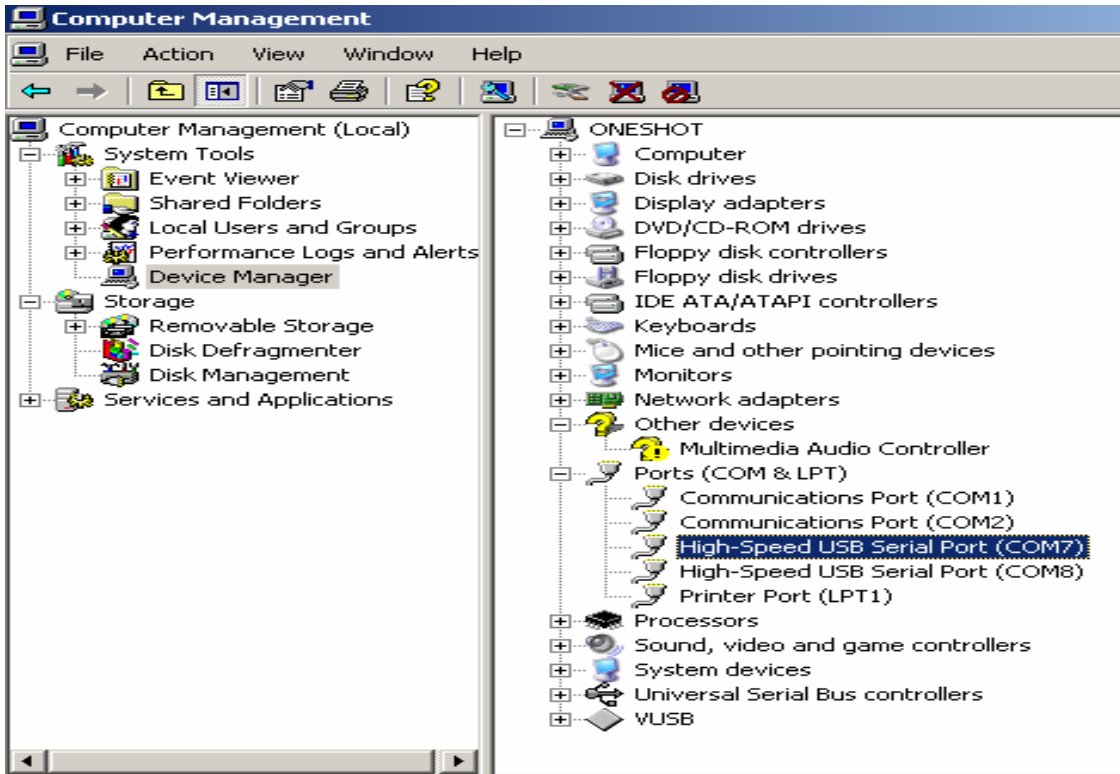
How to set / use “Enable High Baud”

Setting UART Baud Rates under WINDOWS

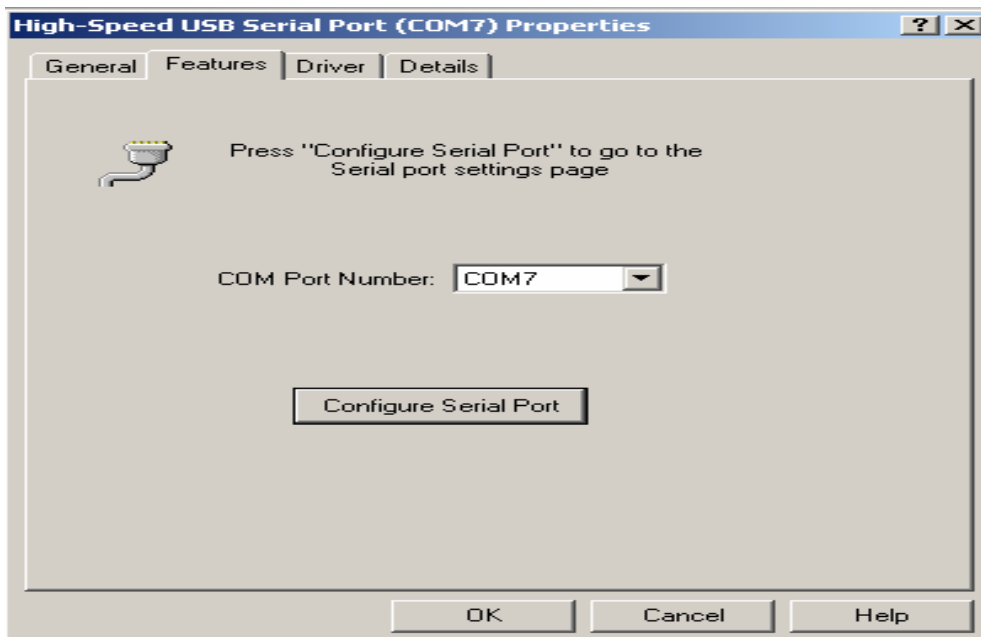
When the windows application opens a COM port application device, it calls a function defined by the driver to set the baud rate. (Eg. Hyper Terminal).

Applications like Hyper Terminal allow the user to select the baud rate up to 921600bps or slower. Therefore it is necessary to supply some extra configuration parameters to allow Hyper Terminal application to be used for High baud rate confirmations. Steps below explain procedure for same.

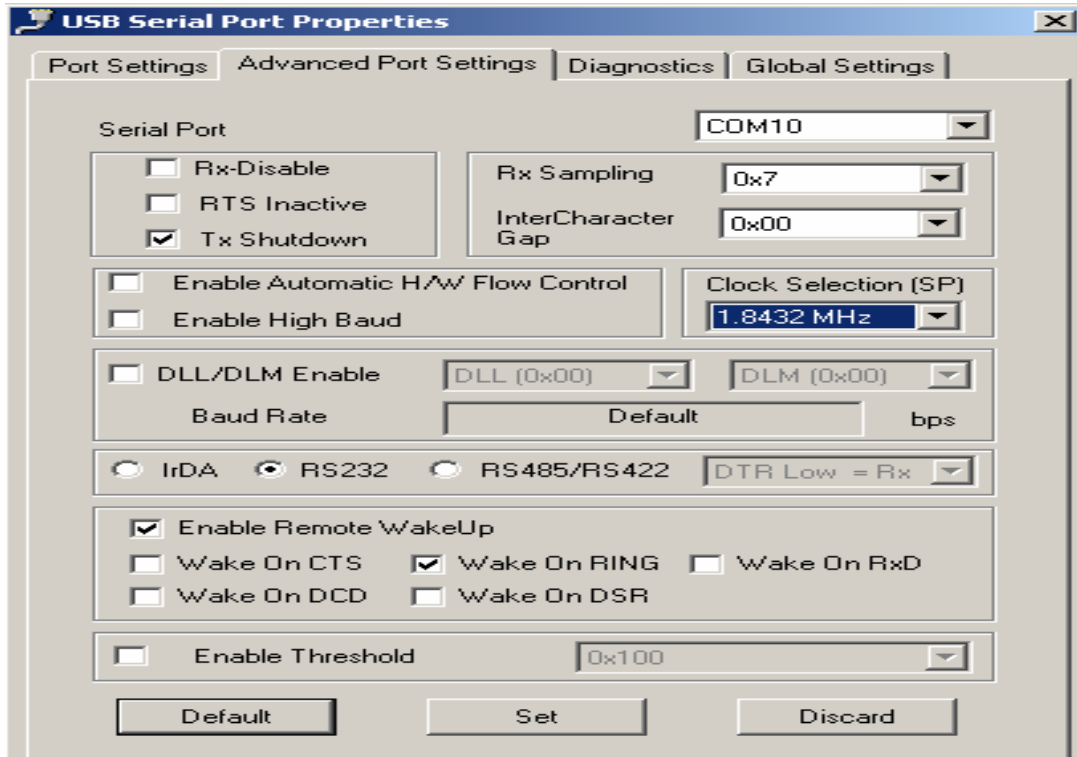
Under Device manager window (as shown in the below) select the port for which the serial baud rates need to be set.



Right Click on High-Speed USB Serial Port(COMX) > Properties > Features. A new window will pop up as shown below. Under normal default operation, driver will ignore the advanced baud rate settings. The driver will set the divisor values as such a 1.8432 MHz crystal is present.



Click on “Configure serial Port”. A pop up window appears as shown below

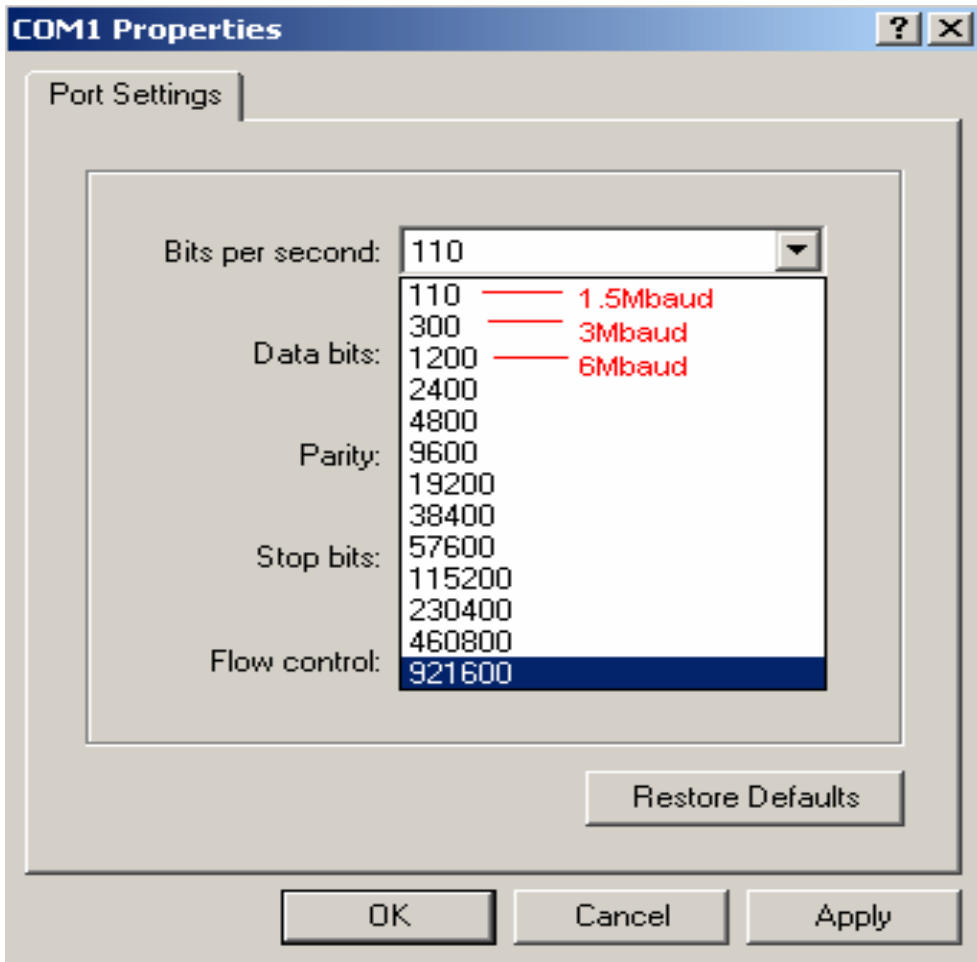


For baud rate support upto 921600 bps “Enable High Baud” option to be left unchecked. For baud rates above 921600 bps this box to be checked for respective serial port.

High baud rate support

To enable baud rate higher than 921600 bps, check “Enable High Baud” option. This will enable to user to select baud rates of 1.5M, 3M and 6Mbps. For setting this baud rates user need to set equivalent bauds as shown below.

Eg : For Hyper Terminal application following baud rates represent higher baud rates when “Enable High Baud” is selected.



Note :- Enable Hard Ware Flow Control in Device manager settings of MCS7840 & also in Hyper Terminal application. And also select Enable High Baud” option for Baud Rates above 921600 bps. (In all conditions)

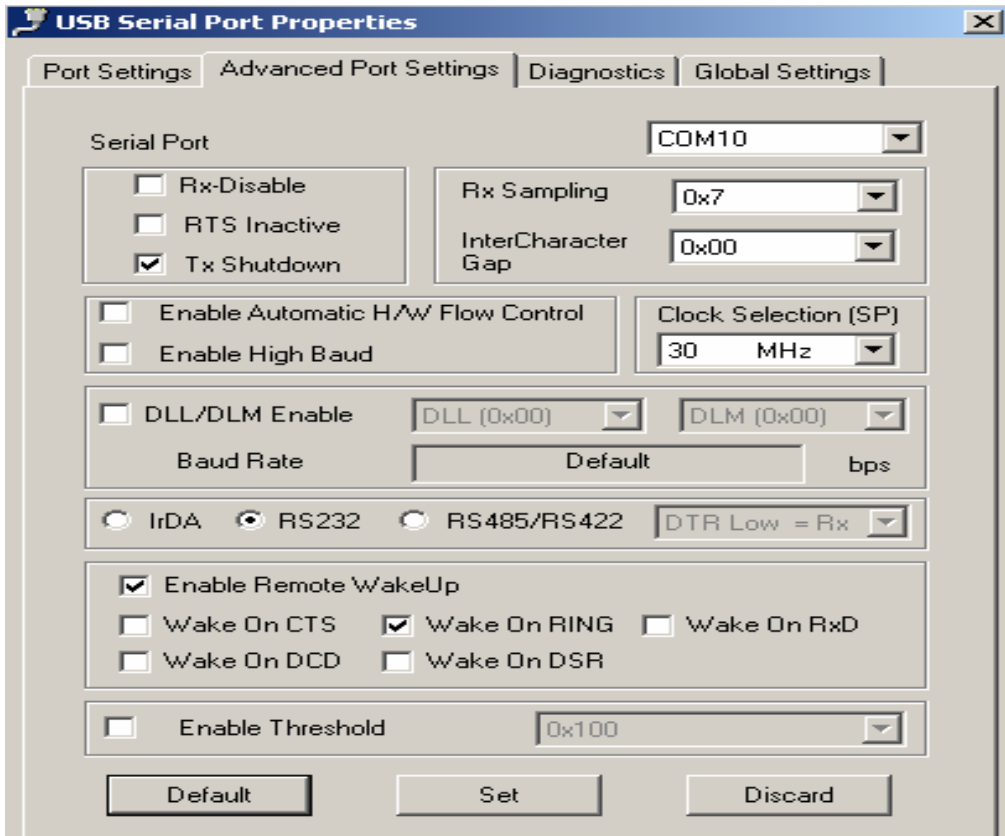
b) Custom baud rates through internal PLL Clock options : Different clock is selected using “clock select” option as shown below. Internal PLL Clock options are 30, 96 & 120 MHz.

Baud clock = Input Clock / 16

Baud rate = Baud clock/ Divisor

Where Divisor = DLL + (256 * DLM).

DLL and DLM values can be seen in Table 1.



If Clock Selection = 30MHz and baud rate selected is 9600baud in terminal application, then the actual set baud will be calculated as below.

Baud Rate = 30 MHz/ 16 * Divisor

From Table 1 : DLL =12, DLM = 0 for 9600 bps. When Clock option is 30Mhz, selection of 9600bps in Hyper Terminal like application supports following custom baud rate.

Divisor = (12+256*0) = 12

Baud Rate = 30MHz/16*12 = 156250baud

Note:- “Enable High Baud” and “DLL/DLM Enable” Options should be disabled for achieving above custom baud rates.

Non-standard baud rates setting through “DLL/DLM Enable”

By selecting the “DLL/DLM Enable” option user can set desired baud rate given by the formula.

Baud rate = input clock/16* Divisor

Divisor = DLL+ (256* DLM)

Input clock source is selected from the “Clock Selection” = 96 MHz. (As shown below)

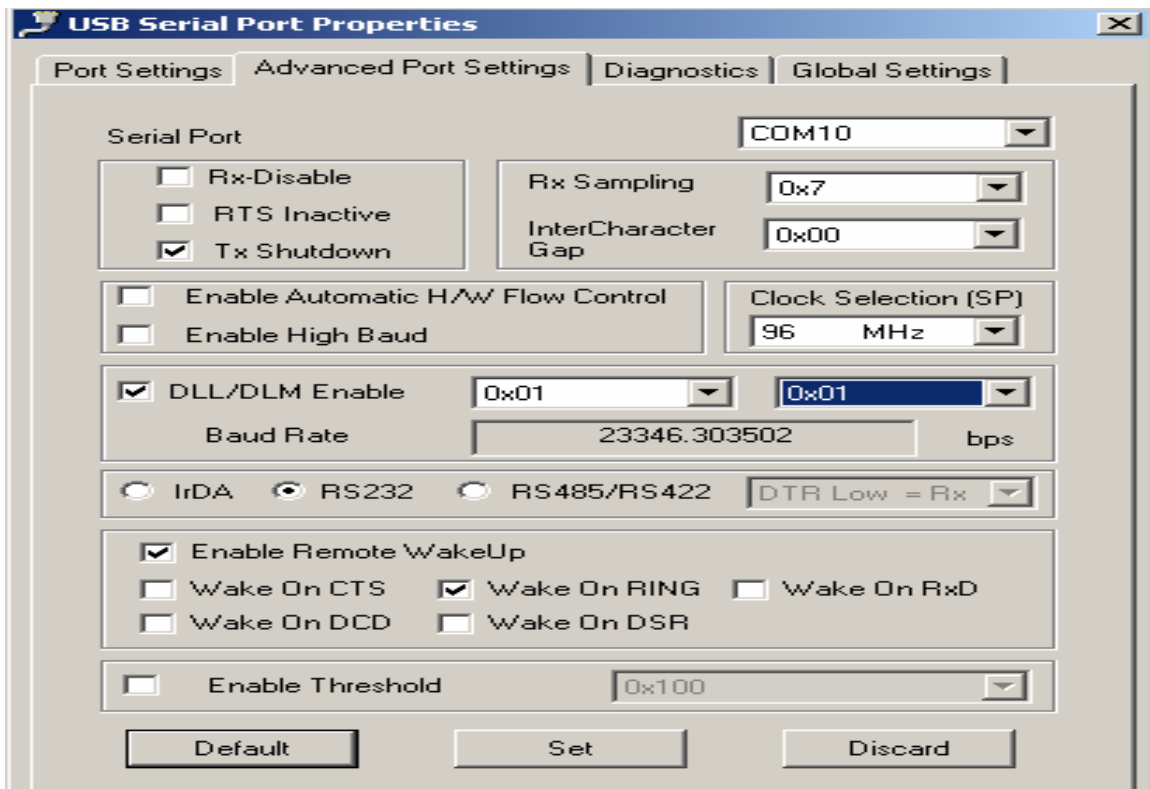
Eg :

If “Clock Selection” = 96MHz and DLL=0x01, DLM= 0x01 then,

Baud rate = 96MHz/16 * Divisor

Divisor = (DLL+ 256*DLM) = 257

Baud rate = 96MHz/16*257 = 23346.6 bps



Important Notes :

i) Once the “DLL/DLM Enable” option box is checked, irrespective of the baud rate selected from the terminal application, baud rate remains unchanged. Same applies when “External Clock” option is selected.

ii) If DLL/DLM Enable is un-checked then Table 1 can be referred for matching custom baud rate through terminal program (based on DLL, DLM settings). Same applies when “External Clock” option is selected.

c) External Clock Mode:

User can give external clock to generate the customized baud rates using this option. By selecting the “DLL/DLM Enable” option user can set desired baud rate given by the formula.

$$\text{Baud rate} = \text{External clk}/16 * \text{Divisor}$$

$$\text{Divisor} = \text{DLL} + (256 * \text{DLM})$$

External clock source can be selected from the “Clock Selection” option, as shown below. Clock source of 5 MHz to 100MHz can be used for external clock source. (Clock source Specs : 5 MHz to 100MHz, Frequency Stability ±30PPM, Duty Cycle - 40/60, Supply Voltage +5V, Output load - 15pF)

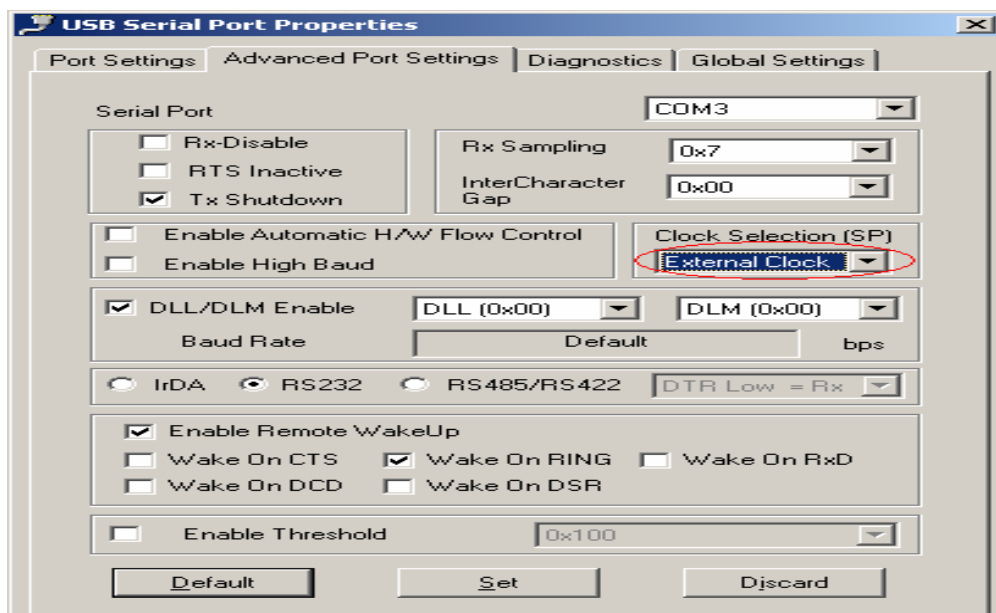
Eg :

If “External clk” = 30MHz and DLL=0x01, DLM= 0x01 then

$$\text{Baud rate} = 30\text{MHz}/16 * \text{Divisor}$$

$$\text{Divisor} = (\text{DLL} + 256 * \text{DLM}) = 257$$

$$\text{Baud rate} = 30\text{MHz}/16 * 257 = 7295 \text{ bps (Approx)}$$



d) PLL OUTPUT mode:

The PLL has two programmable dividers. The “Pre-Divider” (M) divides the Input clock before it goes to the phase comparator. The “Loop-Divider” (N) divides the Output clock signal before it goes to the phase comparator. Together, these two registers are used to set the ratio of the Output clock to Input clock frequencies.

Because they are used as divisors, neither M nor N should be set to zero

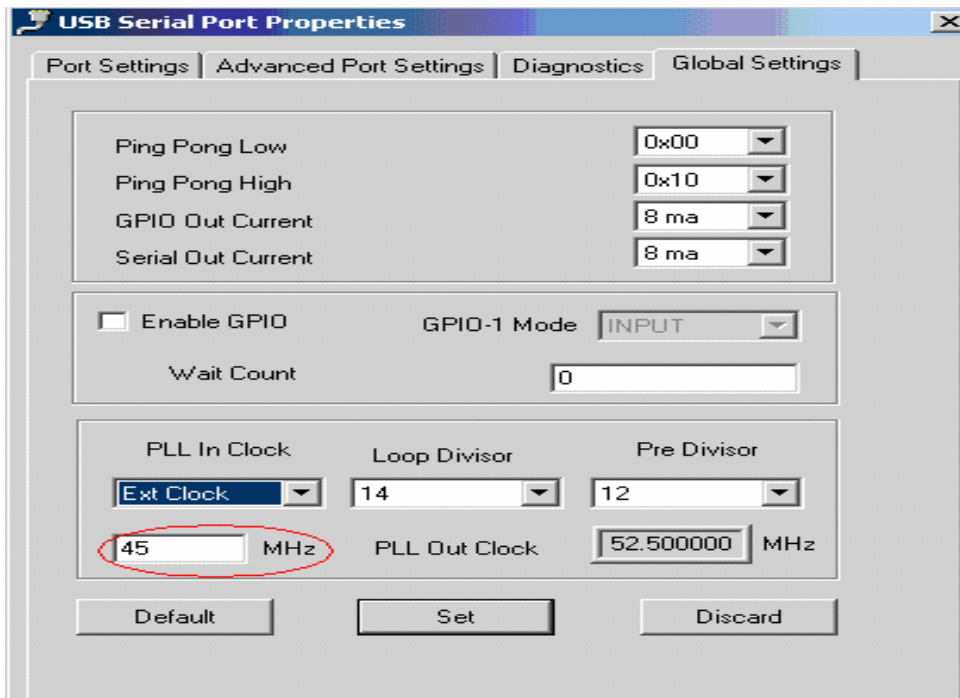
The formula used to set the Output frequency is:

$$F_{Out} = (N/M) * F_{In}$$

In this mode Baud Rate is given by the formula

$$\text{Baud Rate} = [(N/M) * F_{in}] / 16 * \text{Divisor}$$

In order to maintain a stable output clock frequency (FOut), this important relationship must be maintained : 5MHz (Fin/M) 100MHz



“PLL In Clock” can be either 12MHz from crystal or External Clock Source. When “Ext Clock” is selected, user needs to enter the external clock frequency in the box shown above (Red Color) to get the desired output clock from PLL.

Eg : For input External clock of 12MHz, to obtain a 30MHz Output from the PLL, the values M=2 and N=5 are used $((5/2) * 12 = 30)$.

Baud Rate = $[(5/2)*12MHz]/16*Divisor$

Divisor = $DLL + (256*DLM)$

The value of DLL and DLM depends on the baud rate selected in terminal application.

If baud rate selected is 115.2k from the Table 1, $DLL= 1$ and $DLM =0$.

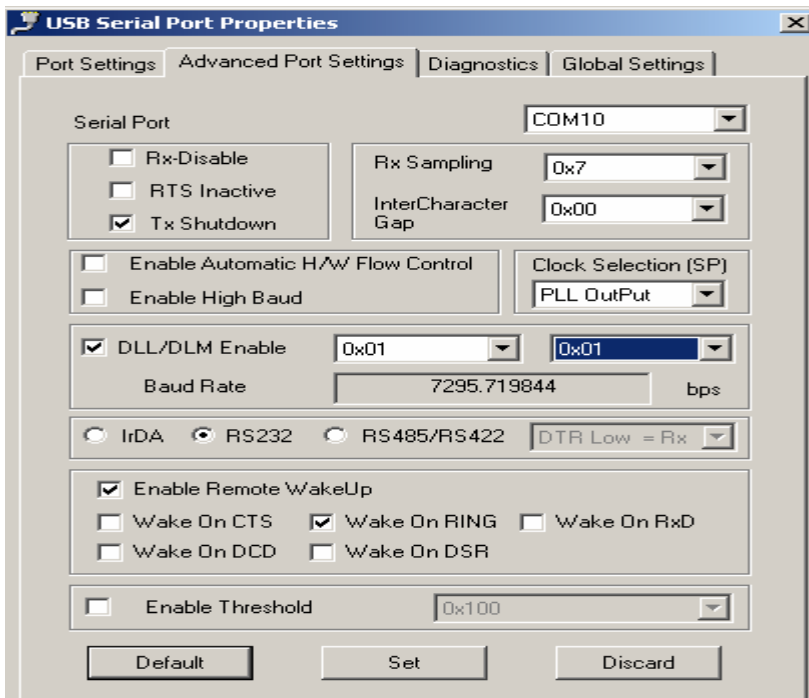
Then Divisor = $1+ (256*0) = 1$, By substituting the Divisor value

Baud Rate =1875000 bps

Note: In this mode “DLL/DLM Enable” option should be disabled by un-checking the box. Select “Enable High Baud” since the baud rate is higher than 921600bps.

Variable Baud Rate using PLL output

If lower baud rates are desired in this mode, “DLL/DLM Enable” option should be enabled as shown in below :



$$\text{Baud Rate} = [(N/M) * \text{Fin}] / (16 * \text{Divisor})$$

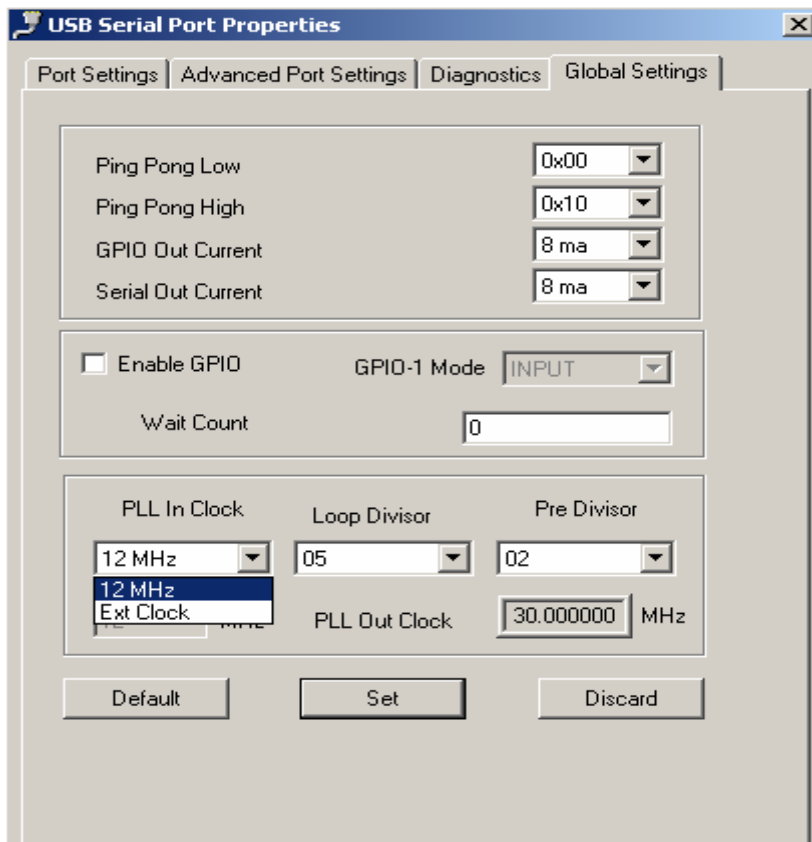
$$\text{Divisor} = \text{DLL} + (256 * \text{DLM})$$

Eg : For input clock of 12MHz, to obtain a 30 MHz Output from the PLL, the values M=2 and N=5 can be used $((5/2) * 12 = 30)$.

$$\text{Baud Rate} = [(5/2) * 12\text{MHz}] / 16 * \text{Divisor}$$

If DLL=0x01 and DLM= 0x01 then,
Divisor = (DLL+ 256*DLM) = 257

$$\begin{aligned} \text{Baud rate} &= 30\text{MHz} / 16 * \text{Divisor} \\ &= 7295 \text{ bps (Approx)} \end{aligned}$$



Custom baud rates can be derived under PLL Out mode through External Clock option also. Either using Table 1 values of DLL, DLM or by Enabling DLL/DLM. M, N values and Clock source value (Frequency) determine Input Frequency.



Application Note For Custom Baud rates

For Additional information: Contact sales@moschip.com for commercial details & techsupport@moschip.com for technical details.

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